REMARKS

Applicant submits this Amendment for consideration in conjunction with a Request for Continued Examination (RCE), and a request for a two-month extension of time. With this Amendment, Applicant amends claims 1, 2, 6, 8, 10, and 16, cancels claim 9, and submits new claims 21 and 22. After entry of this Amendment, claims 1-2, 4-8, and 10-22 will be pending.

With this Amendment, claim 1 has been amended to include the subject matter of claim 9, that is: "the indexing logic is not used for either the ICache portion or TCache portion when the TCache portion is supplying instructions." In the Final Office Action mailed July 21, 2006, the Examiner rejected claim 9 under 35 U.S.C. § 102(e) as allegedly anticipated by Hironaka et al., U.S. Application Publication No. 2004/0088489 ("*Hironaka*"). To further prosecution, Applicant traverses this rejection and submits that *Hironaka* does not teach or suggest all of the elements of claim 1, as amended.

In rejecting claim 9, the Examiner relies on paragraphs 19 and 147 of *Hironaka* and contends that "executing command string in a trace cache is read on this limitation in other words if there is a trace cache hit, traced instructions are executed in a string fashion." However, Applicant respectfully submits that neither the cited portion nor any other portion of *Hironaka* teaches use of an indexing logic. The cited paragraphs generally describe a process of storing an instruction string in a trace cache after the first execution of certain instructions, but no indexing logic is mentioned. Paragraph 19 claims that by storing instructions strings in the trace cache, "fetch efficiency of the processor 1 can be improved," but there is no indication anywhere in *Hironaka* that such

improvement in efficiency is the result of bypassing an indexing logic when the instructions are being supplied from the trace cache.

Hironaka further does not teach or suggest "the indexing logic is not used for either the ICache portion or TCache portion when the TCache portion is supplying instructions," as recited by amended claim 1. In the rejection of claim 8, the Examiner appears to equate the hit judgment circuit of *Hironaka* (see Fig. 13, item 40) with the "indexing logic" of claim 8. (*See* Office Action, page 5, second full paragraph). In *Hironaka*, however, the hit judgment circuit of Fig. 13 is not bypassed under any circumstances. According to paragraphs 136–140 and Fig. 13 of *Hironaka*, the hit judgment circuit is used at all times, including when the instructions are supplied from the trace cache.

In light of these observations, Applicant respectfully submits that claim 1, as amended, is allowable over *Hironaka*. In the Final Office Action, the Examiner also rejected claims 1, 6, 10, and 16 under 35 U.S.C. § 102(b) as allegedly anticipated by Wang et al., U.S. Application Publication No. 2002/0144101 ("*Wang*"). As mentioned above, claim 1 has been amended to include the subject matter formerly of claim 9, which was not rejected under *Wang*. Claim 1, as amended, is therefore allowable over *Wang*.

Claims 6, 10, and 16 have been amended to include a limitation similar to that of claim 9 and therefore are allowable over the cited prior art for at least the same reasons as set forth above with respect to claim 1. Claims 2, 4-5, 7-8, and 11-15, and 17-22 each depend from one of allowable claims 1, 6, 10, or 16, and therefore are also allowable for at least the same reasons.

In view of the foregoing amendments and remarks, Applicant submits that this claimed invention is neither anticipated nor rendered obvious in view of the prior art. Applicant therefore requests reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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GARRETT & DUNNER, L.L.P.

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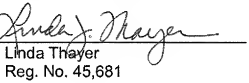
By: 
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